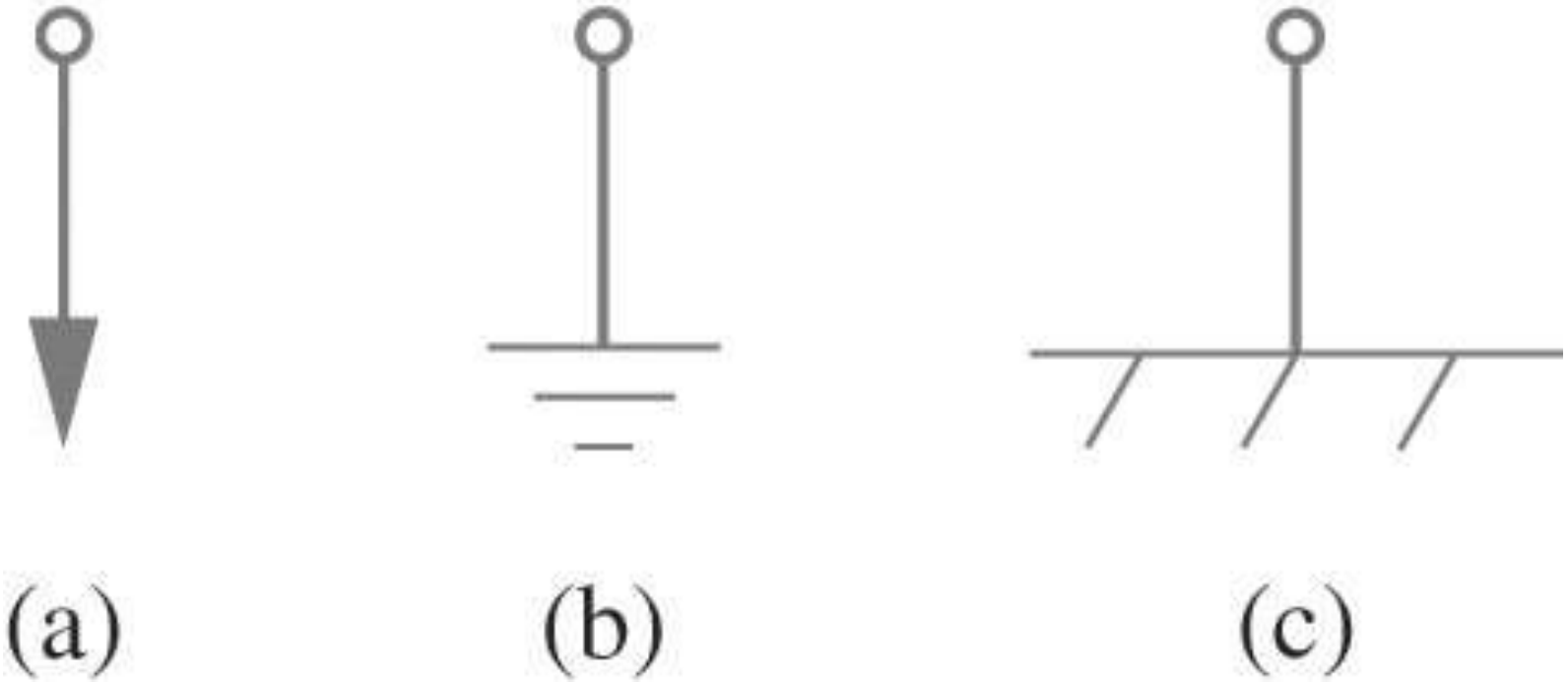
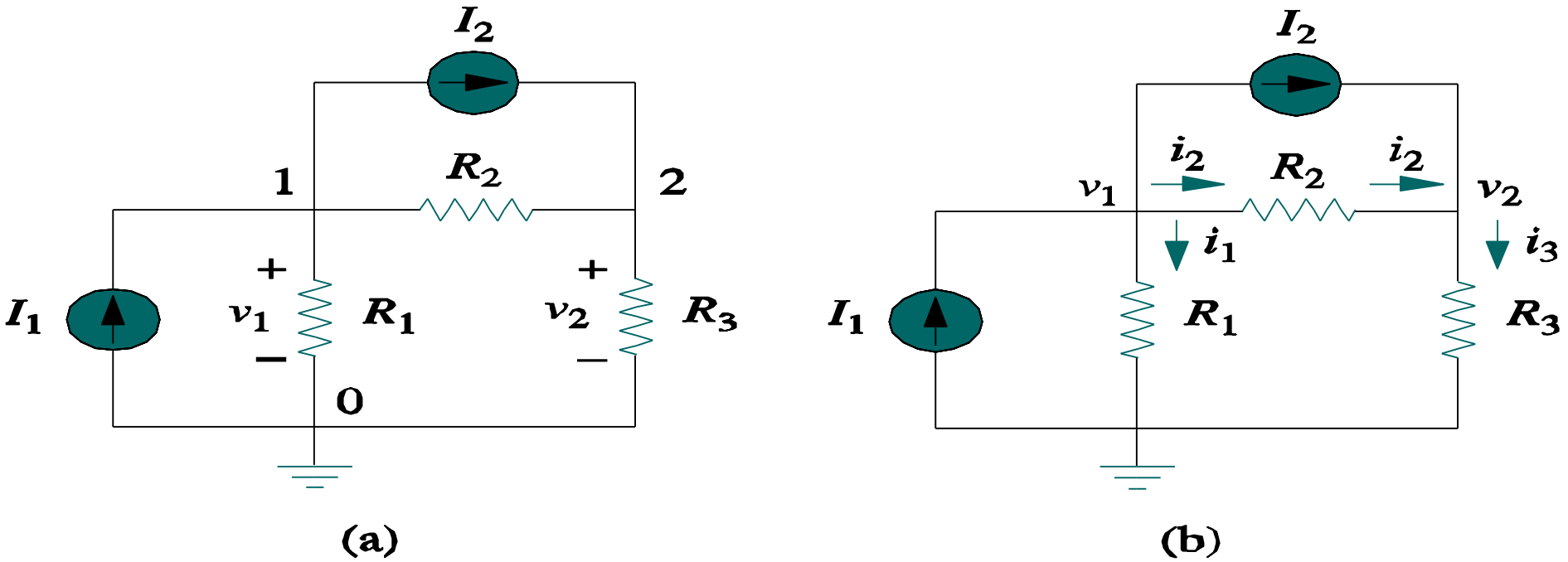
Fig. 3.1 Common symbols for indicating a reference node: (a) common ground, (b) ground, (c) chassis.



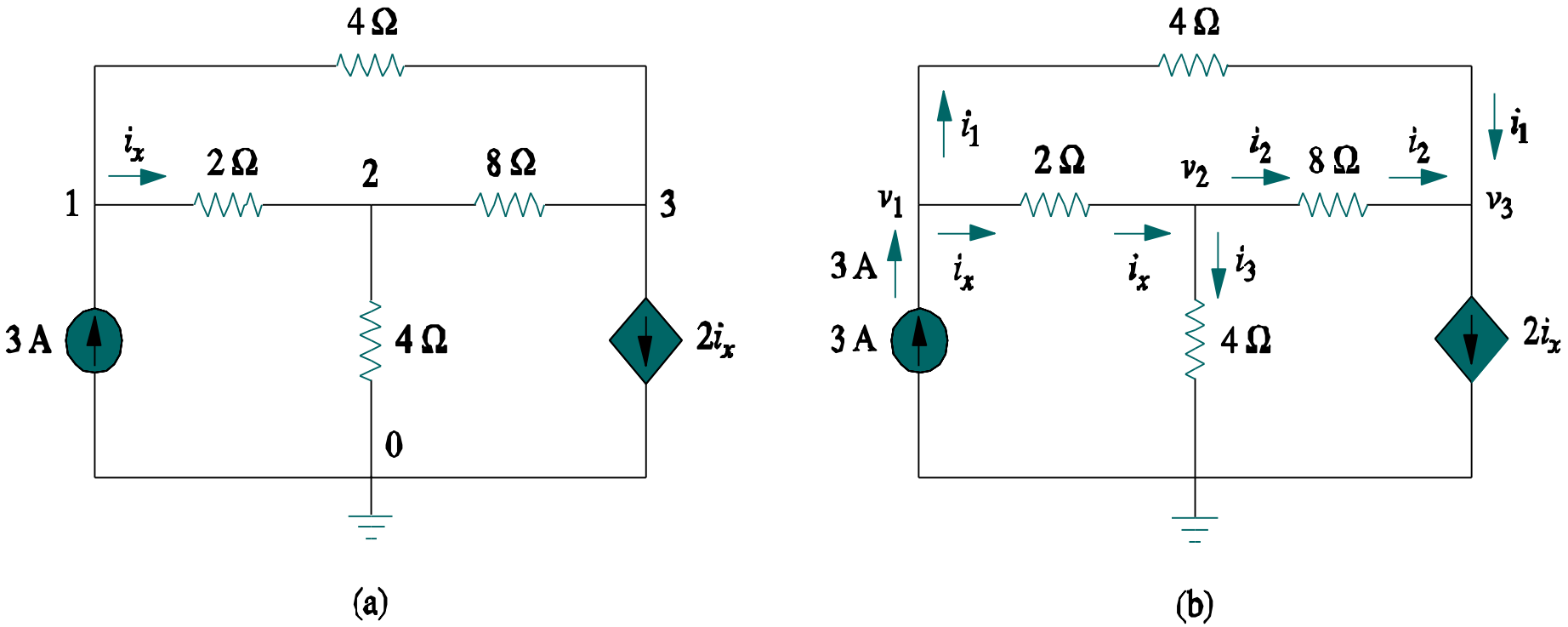
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Fig. 3.2 Typical circuit for nodal analysis



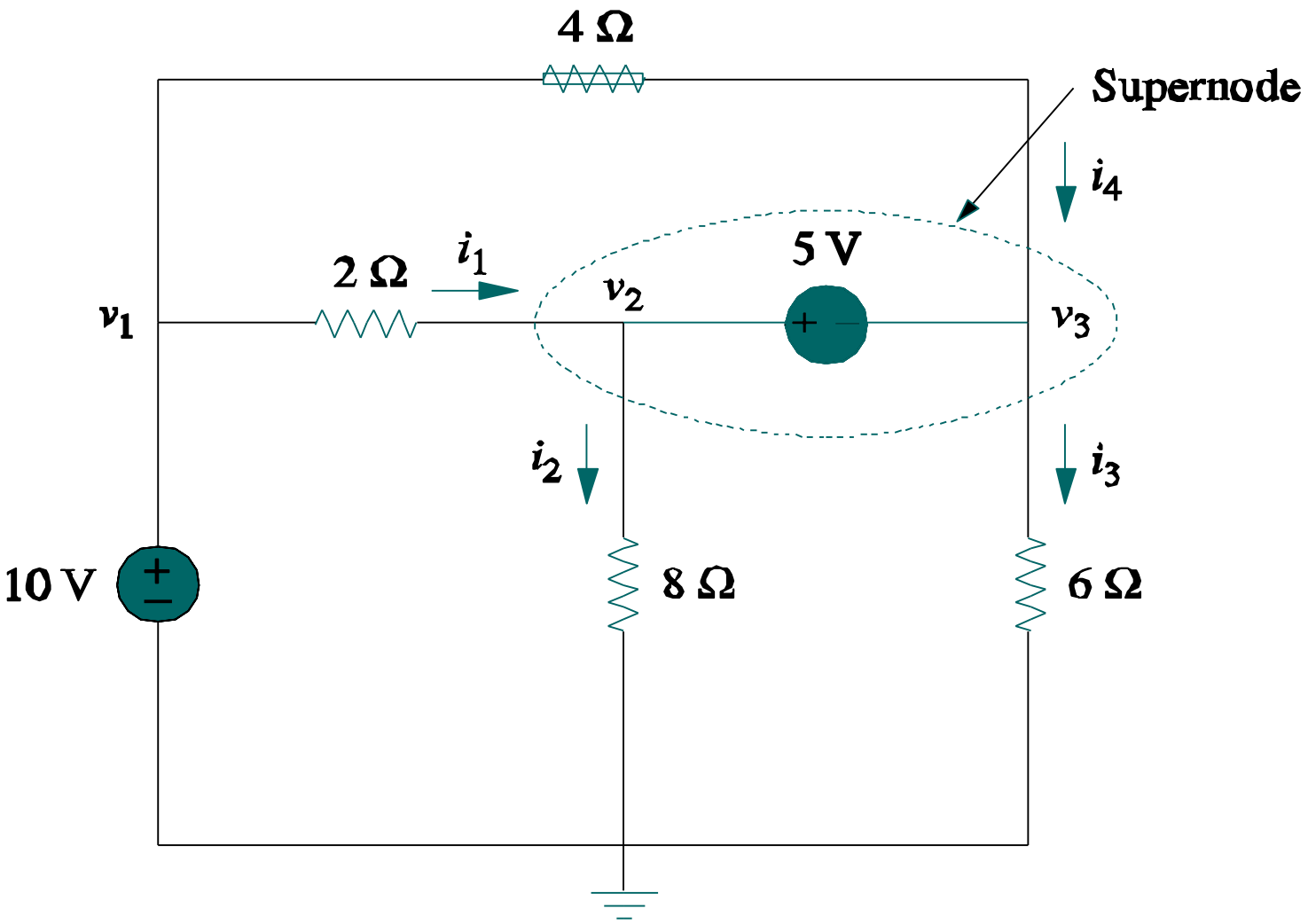
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Fig. 3.5 For Example 3.2: (a) original circuit, (b) circuit for analysis



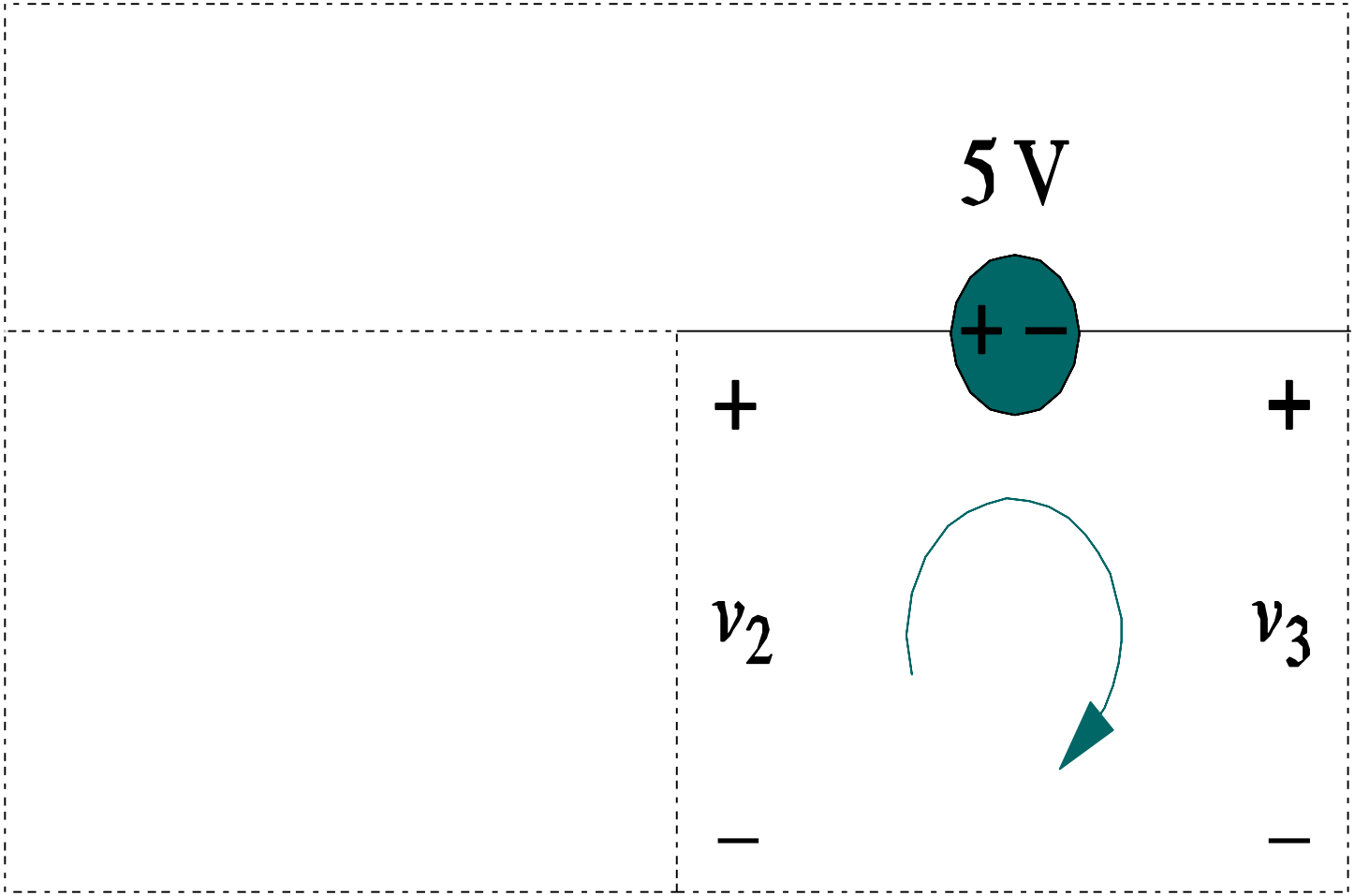
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Fig. 3.7 A circuit with a supernode.



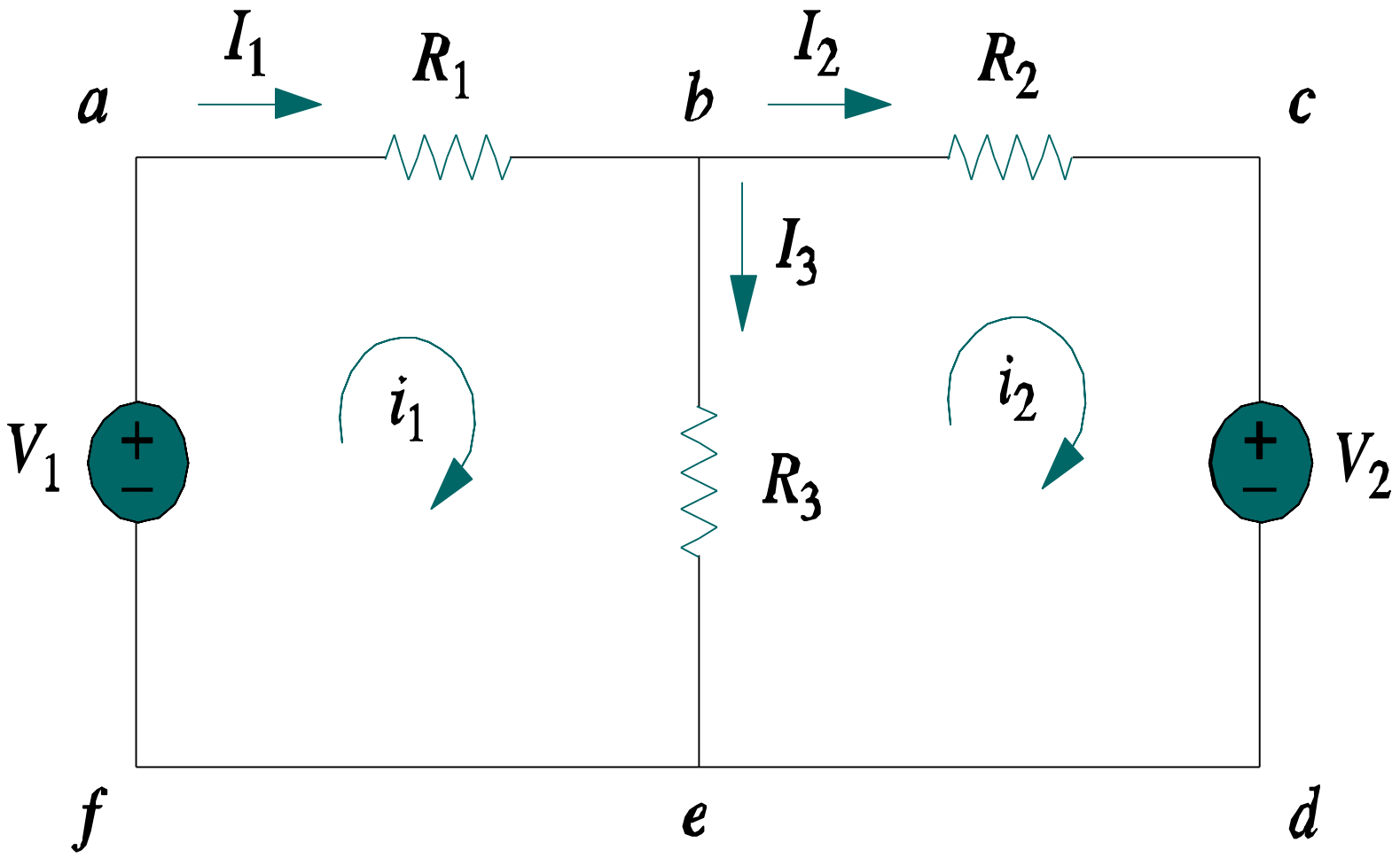
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Fig. 3.8 Applying KVL to a supernode.



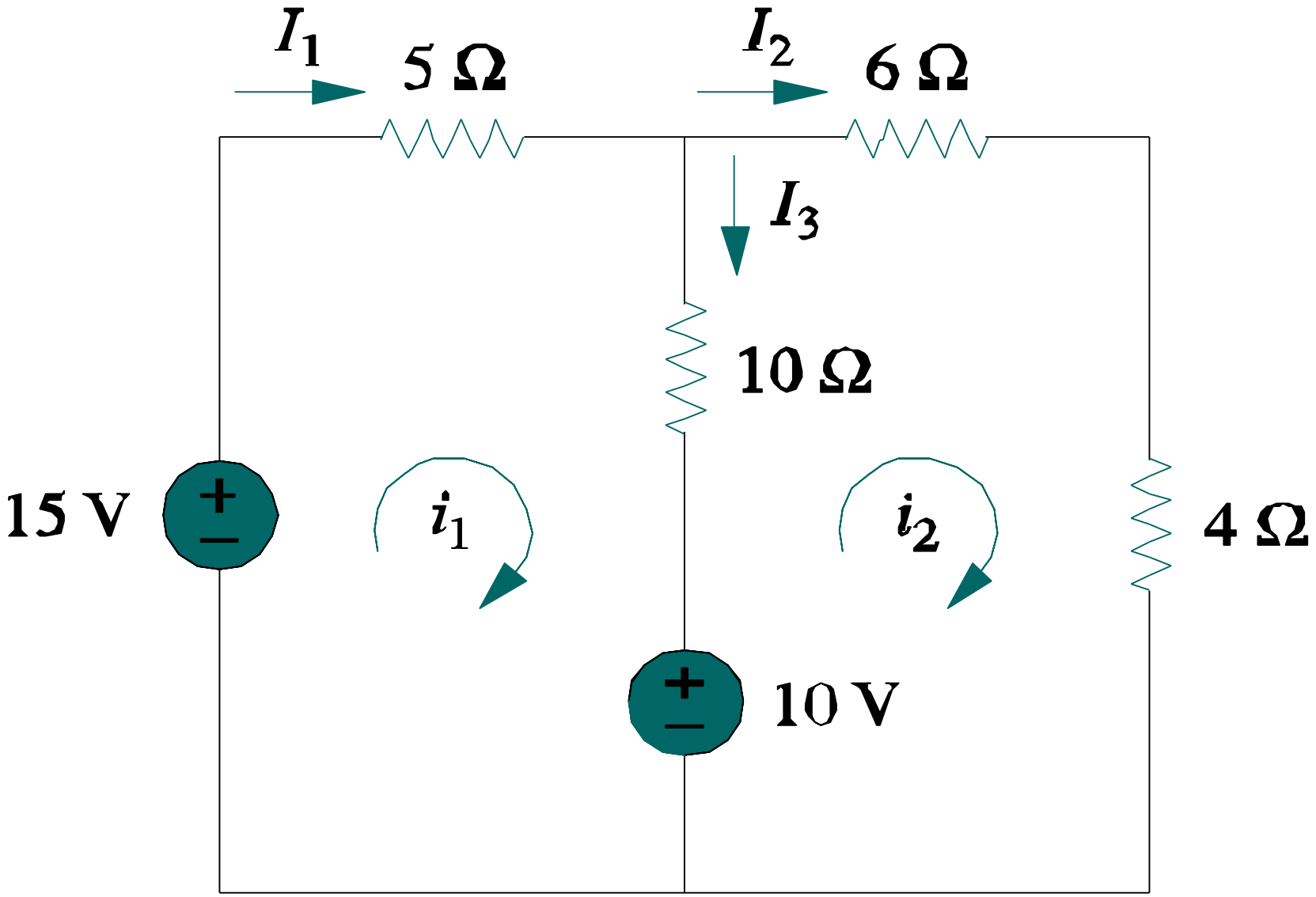
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Fig. 3.17 A circuit with two meshes



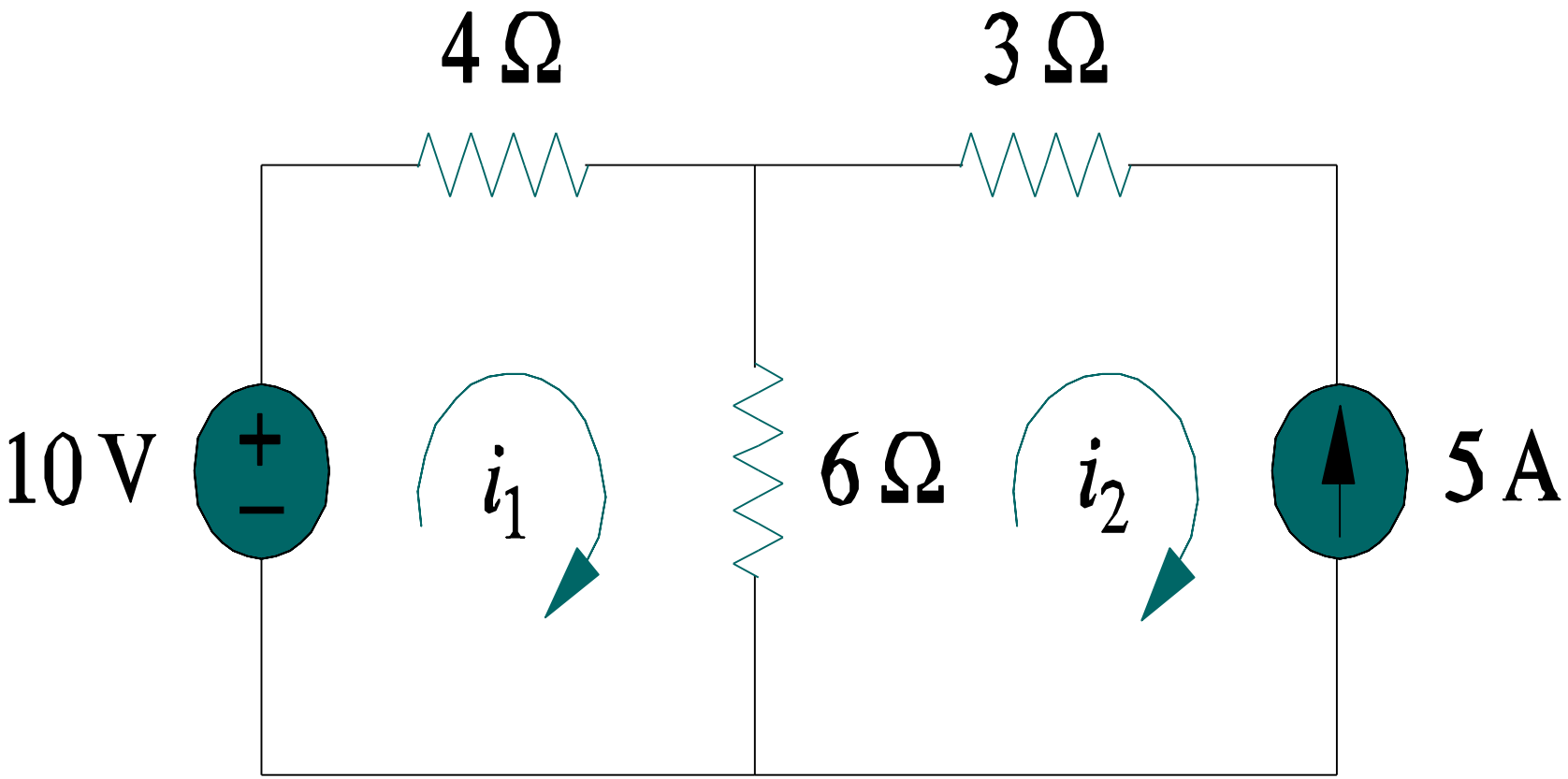
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Fig. 3.18 For Example 3.5



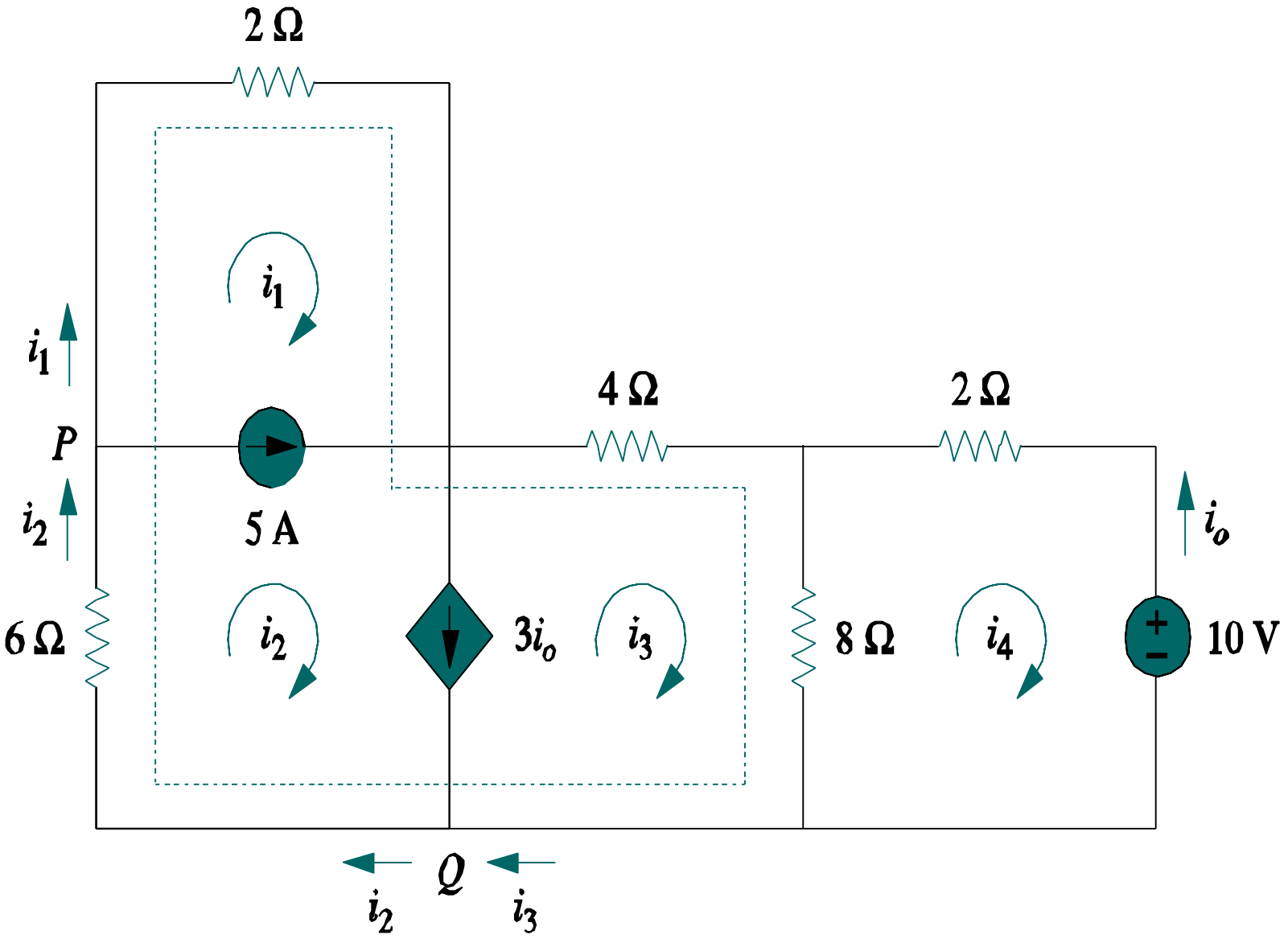
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Fig. 3.22 A circuit with a current source



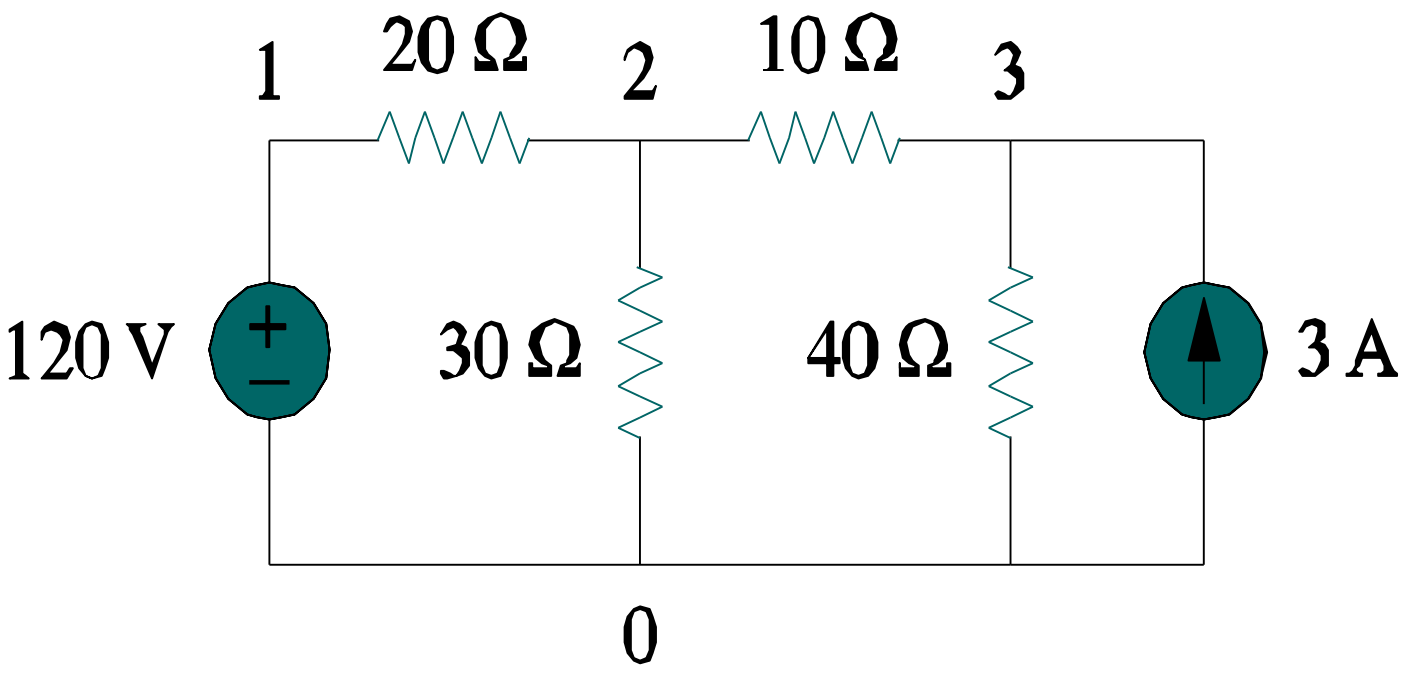
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Fig. 3.24 For Example 3.7



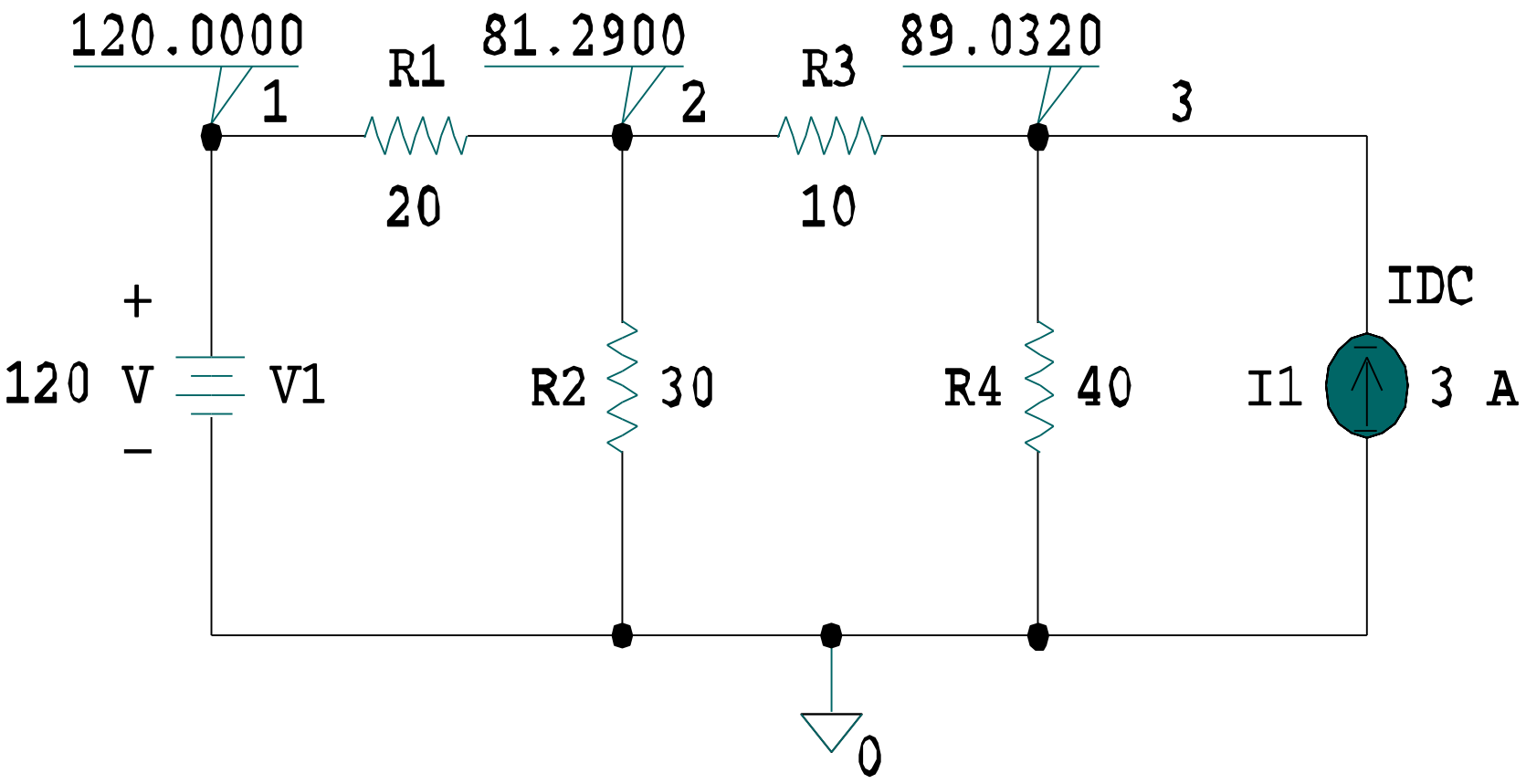
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Fig. 3.31 For Example 3.10



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Fig. 3.32 For Example 3.10; the schematic of the circuit in Fig. 3.31.



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